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B7 Sub C2

3. (Amended) A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, a portion of said gate oxide layer, which is beneath said gate electrode and adjacent said drain region and which defines an overlap region, having an ion implant concentration higher than remaining portions of said oxide layer which is effective to lower the surface electrical field in said overlap region.

4. The circuit structure according to claim 3, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

5. The circuit structure according to claim 3, wherein said source region and said drain region are heavily doped with a second conductivity dopant.

6. The circuit structure according to claim 3, further including a pair of spaces adjacent said gate electrode.

7. The circuit structure according to claim 3, wherein said gate electrode is comprised of polysilicon.

8. The circuit structure according to claim 3, wherein said gate electrode is a gate stack.

9. The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

10. (Amended) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium nitride layer.

11. The circuit structure according to claim 3, further including a pair of conductive studs and an interlevel dielectric layer provided on said semiconductive layer, said interlevel dielectric layer have a pair of throughbores, each accommodating one of each said pair of conductive studs, and one of each said pair of conductive studs contacting one of each said source/drain regions.

12. (Amended) A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, a portion of said gate oxide layer, which is beneath said gate electrode and adjacent said drain region and which defines an overlap region, having an ion implant concentration higher than remaining portions of said gate oxide layer which is effective to lower the surface electrical field in said overlap region; and

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

13. The circuit structure according to claim 12, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

14. (Amended) The circuit structure according to claim 12, wherein a portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.

45. (New) A circuit structure comprising:

a semiconductor layer having a source region, a drain region, and a channel region located between said source/drain regions;

a gate oxide layer located at least on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a portion of said gate oxide layer beneath said gate electrode and adjacent said drain region has a higher ion implant concentration than remaining portions of said gate oxide layer.

46. (New) The circuit structure according to claim 45, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

Remarks

Claim 15-44 were the subject of a restriction requirement and thus have been cancelled. Accordingly, claims 1-14, and 45-46 are pending in the application.

Objection to the Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a). The drawings have been corrected by FIG. 3E, which shows every feature of the claimed invention. Support for FIG. 3E is provided for in the specification and the claims, and thus no new matter has been entered.

Objection to the Specification

The Examiner objected to abstract of the disclosure for reciting a method of making a device, whereas the claims are directed to a device. Accordingly, the abstract has been amended to recite a device of the present invention. Additionally, the disclosure